IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Jun Koyama et al. Art Unit : Unknown
Serial No. : Unassigned Examiner : Unknown
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Title : ELECTRONIC DEVICE AND METHOD OF DRIVING THE SAME

Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Prior to examination, please amend the application as follows:

In the claims:

Amend claims 1-4, 6-14, 16-19, 21-24, 26-29, 31-36, 38-42, 46, 47, 49, 50, 52 and 53 as follows:

1. An electronic device comprising a plurality of pixels, wherein each of the plurality of pixels has a plurality of volatile memory circuits and a plurality of non-volatile memory circuits.

2. A device according to claim 1, wherein the volatile memory circuits are static memories (SRAMs).

3. A device according to claim 1, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

4. A device according to claim 1, wherein the volatile memory circuits are dynamic memories (DRAMs).

6. A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

7. A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

8. A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

9. A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

10. Electronic equipment employing the device according to claim 1.

11. An electronic device comprising a plurality of pixels, wherein:

each of the plurality of pixels has n x m volatile memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal (where n is a natural number, $n \geq 2$); and

each of the plurality of pixels has n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal.

12. A device according to claim 11, wherein the volatile memory circuits are static memories (SRAMs).

13. A device according to claim 11, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

14. A device according to claim 11, wherein the volatile memory circuits are dynamic memories (DRAMs).

16. A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

17. A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

18. A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

19. A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

21. An electronic device comprising a plurality of pixels, each of the pixels having:

a source signal line;

n (where n is a natural number, $n \geq 2$) gate signal lines used for write-in;

n gate signal lines used for read-out;

n transistors used for write-in;

n transistors used for read-out;

n x m volatile memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal;

n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal;

2n volatile memory circuit selection portions;

2n non-volatile memory circuit selection portions;

an electric current supply line;

an EL driver transistor; and

an EL element;

wherein:

gate electrodes of the n write-in transistors are each electrically connected to any one of the n write-in gate signal lines, with each of said gate electrodes connected to a different write-in gate signal line;

input electrodes of the n write-in transistors are each electrically connected to the source signal line;

output electrodes of the n write-in transistors are electrically connected to the volatile memory circuits through any one of the volatile memory circuit selection portions, with each of

said output electrodes being connected through a different volatile memory circuit selection portion;

the output electrodes of the n write-in transistors are electrically connected to the non-volatile memory circuits through any one of the non-volatile memory circuit selection portions, with each of said output electrodes being connected through a different non-volatile memory circuit selection portion;

gate electrodes of the n read-out transistors are each electrically connected to anyone of the n read-out gate signal lines, with each of said gate electrodes connected to a different read-out gate signal line;

the input electrodes of the n write-in transistors are electrically connected to the non-volatile memory circuits through any one of the volatile memory circuit selection portions, with each of said input electrodes being connected through a different volatile memory circuit selection portion;

the input electrodes of the n write-in transistors are electrically connected to the non-volatile memory circuits through any one of the non-volatile memory circuit selection portions, with each of said input electrodes being connected through a different non-volatile selection portion;

the output electrodes of the n write-in transistors are each electrically connected to a gate electrode of the EL driver transistor;

an input electrode of the EL driver transistor is electrically connected to the electric current supply line; and

an output electrode of the EL driver transistor is electrically connected to one electrode of the EL element.

22. A device according to claim 21, wherein the volatile memory circuits are static memories (SRAMs).

23. A device according to claim 21, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

24. A device according to claim 21, wherein the volatile memory circuits are dynamic memories (DRAMs).

26. A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

27. A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

28. A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

29. A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

31. A device according to claim 21, wherein:

the volatile memory circuit selection portions:

select any one circuit from among the volatile memory circuits and the non-volatile memory circuits, make the output electrode of the write-in transistor conductive to the selected one circuit from among the volatile memory circuits and the non-volatile memory circuits, and perform write-in of the digital image signal to the selected one circuit; or

select any one circuit from among the volatile memory circuits and the non-volatile memory circuits, make the input electrode of the write-in transistor conductive to the selected one circuit from among the volatile memory circuits and the non-volatile memory circuits, and perform read-out of the digital image signal from the selected one circuit.

32. A device according to claim 21, wherein the electronic device has:

a shift register for outputting sampling pulses one after another in accordance with a clock signal and a start pulse;

a first latch circuit for storing the n-bit digital image signal (where n is a natural number, $n \geq 2$) in accordance with the sampling pulse;

a second latch circuit into which the n-bit digital image signal stored in the first latch circuit is transferred; and

a bit selection circuit for selecting, in order, single bits of the n-bit digital image signal transferred to the second latch circuit, and outputting the selected single bits to the source signal line.

33. An electronic device comprising a plurality of pixels, each of the pixels having:

n (where n is a natural number, $n \geq 2$) source signal lines;

n gate signal lines used for write-in;

n gate signal lines used for read-out;

n transistors used for write-in;

n transistors used for read-out;

n x m volatile memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal;

n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal;

2n volatile memory circuit selection portions;

2n non-volatile memory circuit selection portions;

an electric current supply line;

an EL driver transistor; and

an EL element;

wherein:

gate electrodes of the n write-in transistors are each electrically connected to any one of the write-in gate signal lines, with each of said gate electrodes being connected to a different write-in gate signal line;

input electrodes of the n write-in transistors are each electrically connected to any one of the sources signal lines, with each of said input electrodes being connected to a different source signal line;

output electrodes of the n write-in transistors are electrically connected to volatile memory circuits through any one of the volatile memory circuit selection portions, with each of said output electrodes being connected through a different volatile memory circuit selection portion;

the output electrodes of the n write-in transistors are electrically connected to the non-volatile memory circuits through any one of the non-volatile memory circuit selection portions, with each of said output electrodes being connected through a different non-volatile memory circuit selection portion;

gate electrodes of the n read-out transistors are each electrically connected to any one of the n read-out gate signal lines, with each of said gate electrodes being connected to a different read-out gate signal line;

input electrodes of the n read-out transistors are electrically connected to the non-volatile memory circuits through any one of the volatile memory circuit selection portions, with each of said input electrodes being connected through a different volatile memory circuit selection portion;

the input electrodes of the n read-out transistors are electrically connected to the non-volatile memory circuits through any one of the non-volatile memory circuit selection portions, with each of said input electrodes being connected through a different non-volatile selection portion;

the output electrodes of the n write-in transistors are each electrically connected to a gate electrode of the EL driver transistor;

an input electrode of the EL driver transistor is electrically connected to the electric current supply line; and

an output electrode of the EL driver transistor is electrically connected to one electrode of the EL element.

34. A device according to claim 33, wherein the volatile memory circuits are static memories (SRAMs).

35. A device according to claim 33, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

36. A device according to claim 33, wherein the volatile memory circuits are dynamic memories (DRAMs).

38. A device according to claim 33, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

39. A device according to claim 33, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

40. A device according to claim 33, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

41. A device according to claim 33, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

42. A device according to claim 33, wherein:

the memory circuit selection portions:

select any one circuit from among the volatile memory circuits and the non-volatile memory circuits, make the output electrode of the write-in transistor conductive to the selected one circuit from among the volatile memory circuits and the non-volatile memory circuits, and perform write-in of the digital image signal to the selected one circuit; or

select any one circuit from among the volatile memory circuits and the non-volatile memory circuits, make the input electrode of the write-in transistor conductive to the selected

one circuit from among the volatile memory circuits and the non-volatile memory circuits, and perform read-out of the digital image signal from the selected one circuit.

46. A method of driving an electronic device for performing display of an image using an n-bit digital image signal (where n is a natural number, $n \geq 2$), wherein the electronic device has a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels, the method comprising:

in the source signal line driver circuit, outputting a sampling pulse from a shift register and inputting the sampling pulse to a latch circuit, storing the digital image signal in the latch circuit in accordance with the sampling pulse, and writing the stored digital image signal to a source signal line;

in the gate signal line driver circuit, outputting a gate signal line selection pulse and selecting a gate signal line; and

in the plurality of pixels, in a row in which the gate signal line is selected, writing the n-bit digital image signal input from the source signal line to a memory circuit, reading the n-bit digital image signal stored in the memory circuit, writing the n-bit digital image signal input from the source signal line or the n-bit digital image signal stored in the memory circuit to a non-volatile memory circuit, reading the n-bit digital image signal stored in the non-volatile memory circuit, or writing the n-bit digital image signal stored in the non-volatile memory circuit to the memory circuit.

47. A method according to claim 46, further comprising, in a static image display period, stopping the source signal line driver circuit by repeatedly reading out the n-bit digital image signal stored in the memory circuit to display a static image.

49. A method of driving an electronic device for performing display of an image using an n-bit digital image signal (where n is a natural number, $n \geq 2$), wherein the electronic device has a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels, the method comprising:

in the source signal line driver circuit, outputting a sampling pulse from a shift register and inputting the sampling pulse to a latch circuit, storing the digital image signal in the latch circuit in accordance with the sampling pulse, and writing the stored digital image signal to a source signal line;

outputting from the gate signal line driver circuit a gate signal line selection pulse to select gate signal lines in order from a first row; and

in the plurality of pixels, writing the n-bit digital image signal in order from the first row or reading the n-bit digital image signal.

50. A method according to claim 49, further comprising, in a static image display period, stopping the source signal line driver circuit by repeatedly reading out the n-bit digital image signal stored in the memory circuit to display a static image.

52. A method of driving an electronic device for performing display of an image using an n-bit image signal (where n is a natural number, $n \geq 2$), wherein the electronic device has a source signal line driver circuit, a gate signal line driver circuit, and a plurality of pixels, the method comprising:

in the source signal line driver circuit, outputting a sampling pulse from a shift register and inputting the sampling pulse to a latch circuit, storing the digital image signal in the latch circuit in accordance with the sampling pulse, and writing the stored digital image signal to a source signal;

the gate signal line driver circuit specifying an arbitrary row of gate signal lines and outputting a gate signal line selection pulse; and

in the plurality of pixels, writing the n-bit digital image signal in the specified arbitrary row of the gate signal lines or reading the n-bit digital image signal.

53. A method according to claim 52, further comprising, in a static image display period, stopping the source signal line driver circuit by repeatedly reading out the n-bit digital image signal stored in the memory circuit to display a static image.

REMARKS

The amendments to the claims made herein are to correct minor grammatical errors and to place the application in better form for examination. No new matter is added.

Attached is a marked-up version of the changes being made by the current amendment.

Applicants ask that all claims be examined. Please apply any charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Version with markings to show changes made

In the claims:

Claims 1-4, 6-14, 16-19, 21-24, 26-29, 31-36, 38-42, 46, 47, 49, 50, 52 and 53 have been amended as follows:

1. (Amended) An electronic device comprising a plurality of pixels, wherein each of the plurality of pixels has a plurality of volatile memory circuits and a plurality of non-volatile memory circuits.

2. (Amended) A device according to claim 1, wherein the volatile memory circuits are static memories (SRAMs).

3. (Amended) A device according to claim 1, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

4. (Amended) A device according to claim 1, wherein the volatile memory circuits are dynamic memories (DRAMs).

6. (Amended) A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

7. (Amended) A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

8. (Amended) A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

9. (Amended) A device according to claim 1, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

10. (Amended) Electronic equipment employing the **[electronic]** device according to claim 1.

11. (Amended) An electronic device comprising a plurality of pixels, wherein:

each of the plurality of pixels has n x m volatile memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal (where n is a natural number, $n \geq 2$); and

each of the plurality of pixels has n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal.

12. (Amended) A device according to claim 11, wherein the volatile memory circuits are static memories (SRAMs).

13. (Amended) A device according to claim 11, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

14. (Amended) A device according to claim 11, wherein the volatile memory circuits are dynamic memories (DRAMs).

16. (Amended) A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

17. (Amended) A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

18. (Amended) A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

19. (Amended) A device according to claim 11, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

21. (Amended) An electronic device comprising a plurality of pixels, each of the pixels having:

a source signal line;

n (where n is a natural number, $n \geq 2$) gate signal lines used for write-in;

n gate signal lines used for read-out;

n transistors used for write-in;

n transistors used for read-out;

n x m volatile memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal;

n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal;

2n volatile memory circuit selection portions;

2n non-volatile memory circuit selection portions;

an electric current supply line;

an EL driver transistor; and

an EL element;

wherein:

gate electrodes of the n write-in transistors are each electrically connected to any one of the n write-in gate signal lines, with each of said gate electrodes connected to a different write-in gate signal line;

input electrodes of the n write-in transistors are each electrically connected to the source signal line;

output electrodes of the n write-in transistors are electrically connected to the **[m]** volatile memory circuits through any one of the **[n]** volatile memory circuit selection portions, with each of said output electrodes being connected through a different volatile memory circuit selection portion;

the output electrodes of the n write-in transistors are electrically connected to the **[k]** non-volatile memory circuits through any one of the **[n]** non-volatile memory circuit selection portions, with each of said output electrodes being connected through a different non-volatile memory circuit selection portion;

gate electrodes of the n read-out transistors are each electrically connected to any one of the n read-out gate signal lines, with each of said gate electrodes connected to a different read-out gate signal line;

the input electrodes of the n write-in transistors are electrically connected to the **[k]** non-volatile memory circuits through any one of the **[n]** volatile memory circuit selection portions, with each of said in put electrodes being connected through a different volatile memory circuit selection portion;

the input electrodes of the n write-in transistors are electrically connected to the **[k]** non-volatile memory circuits through any one of the **[n]** non-volatile memory circuit selection portions, with each of said input electrodes being connected through a different non-volatile selection portion;

the output electrodes of the n write-in transistors are each electrically connected to a gate electrode of the EL driver transistor;

an input electrode of the EL driver transistor is electrically connected to the electric current supply line; and

an output electrode of the EL driver transistor is electrically connected to one electrode of the EL element.

22. (Amended) A device according to claim 21, wherein the volatile memory circuits are static memories (SRAMs).

23. (Amended) A device according to claim 21, wherein the volatile memory circuits are ferroelectric memories (FeRAMs).

24. (Amended) A device according to claim 21, wherein the volatile memory circuits are dynamic memories (DRAMs).

26. (Amended) A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed over a glass substrate.

27. (Amended) A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed over a plastic substrate.

28. (Amended) A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed over a stainless steel substrate.

29. (Amended) A device according to claim 21, wherein the volatile and non-volatile memory circuits are formed on a single crystal wafer.

31. (Amended) A device according to claim 21, wherein:

the volatile memory circuit selection portions:

select any one circuit from among the **[m]** volatile memory circuits and the **[k]** non-volatile memory circuits, make the output electrode of the write-in transistor conductive to the selected one circuit from among the **[m]** volatile memory circuits and the **[k]** non-volatile memory circuits, and perform write-in of the digital image signal to the selected one circuit; or

select any one circuit from among the **[m]** volatile memory circuits and the **[k]** non-volatile memory circuits, make the input electrode of the write-in transistor conductive to the selected one circuit from among the **[m]** volatile memory circuits and the **[k]** non-volatile memory circuits, and perform read-out of the digital image signal from the selected one circuit.

32. (Amended) A device according to claim 21, wherein the electronic device has:

a shift register for outputting sampling pulses one after another in accordance with a clock signal and a start pulse;

a first latch circuit for storing the n-bit digital image signal (where n is a natural number, $n \geq 2$) in accordance with the sampling pulse;

a second latch circuit into which the n-bit digital image signal stored in the first latch circuit is transferred; and

a bit selection circuit for selecting, in order, **[one bit portions]** single bits of the n-bit digital image signal transferred to the second latch circuit, and outputting the selected single bits to the source signal line.

33. (Amended) An electronic device comprising a plurality of pixels, each of the pixels having:

n (where n is a natural number, n 2) source signal lines;

n gate signal lines used for write-in;

n gate signal lines used for read-out;

n transistors used for write-in;

n transistors used for read-out;

n x m volatile memory circuits for storing m frame portions (where m is a natural number, $m \geq 1$) of an n-bit digital image signal;

n x k non-volatile memory circuits for storing k frame portions (where k is a natural number, $k \geq 1$) of the n-bit digital image signal;

2n volatile memory circuit selection portions;

2n non-volatile memory circuit selection portions;

an electric current supply line;

an EL driver transistor; and

an EL element;

wherein:

gate electrodes of the n write-in transistors are each electrically connected to any one of the write-in gate signal lines, with each of said gate electrodes being connected to a different write-in gate signal line;

input electrodes of the n write-in transistors are each electrically connected to any one of the sources signal lines, with each of said input electrodes being connected to a different source signal line;

output electrodes of the n write-in transistors are electrically connected to **[m]** volatile memory circuits through any one of the **[n]** volatile memory circuit selection portions, with each of said output electrodes being connected through a different volatile memory circuit selection portion;

the output electrodes of the n write-in transistors are electrically connected to the **[k]** non-volatile memory circuits through any one of the **[n]** non-volatile memory circuit selection portions, with each of said output electrodes being connected through a different non-volatile memory circuit selection portion;

gate electrodes of the n read-out transistors are each electrically connected to any one of the n read-out gate signal lines, with each of said gate electrodes being connected to a different read-out gate signal line;

input electrodes of the n read-out transistors are electrically connected to the **[k]** non-volatile memory circuits through any one of the **[n]** volatile memory circuit selection portions, with each of said input electrodes being connected through a different volatile memory circuit selection portion;

the input electrodes of the n read-out transistors are electrically connected to the **[k]** non-volatile memory circuits through any one of the **[n]** non-volatile memory circuit selection portions, with each of said input electrodes being connected through a different non-volatile selection portion;